In the Specification

Please replace paragraph 8 with the following marked up paragraph:

--The operation of one embodiment of a binary translator according to the invention is described by reference to Figure 1. As part of the process of translating code from a source to a target architecture, the binary translator 101 generates an instruction that maps multiple distinct exception masks 103, 105 in the source architecture into a single equivalent exception mask 107 in the target architecture. The code block 109 is executed in a "regular" execution mode 111. Assuming all exceptions are masked, or if no exceptions are raised, the regular execution mode execution completes and the binary translator 101 begins translating the next source code block.--

Please replace paragraph 11 with the following marked up paragraph:

--To determine the correct state, the binary translator restores the state of the source architecture to the pre-instruction state 113, and re-translates and executes the excepted instruction in an "exception rerun" mode 119 that generates the state of source architecture. In the embodiment of the exception rerun mode illustrated in Figure 1, the binary translator 101 generates an instruction that sets the target exception mask 107 to an exception mask 115 that prevents the generation of all exceptions so that all translated instructions will be executed, and the post-instruction state can be established.--

Pleaser replace paragraph 20 with the following marked up paragraph:

-- It will be appreciated that the optimization described above may be embodied in binary translators that do not incorporated the exception masking of the present invention.--